

Memory Size Estimation for Multimedia Applications*

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Abstract

Memory modules dominate the cost, performance, and power of embedded systems that process multidimensional signals, typically present in image and video processing. Therefore, studying the impact of parallelism on memory size is crucial for trading off system performance against area cost, to enable intelligent system partitioning and exploration. We propose a memory size estimation method for algorithmic specifications containing multidimensional arrays and parallel constructs, intended as part of a high-level partitioning and exploration methodology. The system designer can trade-off estimation accuracy for increased run time. We present the results of our estimation approach on a number of image and video processing kernels, and discuss some preliminary results on the influence of parallelism on storage requirement.

1 Introduction

In the design of embedded HW/SW systems, the high level design space exploration step is critical for obtaining a cost effective implementation. Decisions at this level have the highest impact on the final result. The step of partitioning the initial specification into HW/SW, as well as between different processing units, together with decisions regarding the parallelism inherent in such designs, allow trading-off the system performance against cost. To drive this process, a set of fast estimation tools is crucial.

Varying the code parallelism by means of code transformations [2] (e.g., instruction reordering, loop splitting, fusion, fission, interchanging, skewing [14]), or by assigning code portions to different partitions, may result in significant performance variations for the system implementation. More instructions executed in parallel lead usually to higher performance, but hardware cost may grow substantially.

In the algorithmic specifications of image and video applications the multidimensional variables (signals) are the main data structures. These large arrays of signals have to be stored in on-chip and off-chip memories. In such applications, memory often proves to be the most important hardware resource. Therefore it is important to be able to predict after a set of (parallelizing) transformations and partitioning steps the memory requirements for every design alternative.

We propose a method for memory size estimation, targeting specifications with multidimensional arrays, containing both instruction level (fine-grain) and coarse-

grain parallelism [2], [14]. The impact of parallelism on memory size has not been previously studied in a consistent way. Together with tools for estimating the area of functional units and the performance of the design, our memory estimation approach can be used in a high level exploration methodology to trade-off performance against system cost.

Our paper is organized as follows. Section 2 briefly reviews some major results obtained in the field of memory estimation. Section 3 defines the memory size estimation problem. Our approach is presented in Section 4. In Section 5 we discuss the influence of parallelism on memory size. Our experimental results are summarized in Section 6, followed by the conclusions and our future directions of research in Section 7.

2 Previous work

One of the earliest approaches to memory estimation is the left edge algorithm [5], which assigns the scalar variables to registers. This approach is not suited for multidimensional signal processing applications, due to the prohibitive computational effort.

One of the earliest approaches of handling arrays of signals is based on clustering the arrays into memory modules such that a cost function is minimized [9]. The possibility of signals with disjoint life times to share common storage locations is however ignored, the resulting memory requirements often significantly exceeding the actual storage needed. More recently, [10] proposed a more refined array clustering, along with a technique for binding groups of arrays to memory modules drawn from a given library. However, it seems that the technique does not perform in-place mapping within an array.

Approaches which deal with large multidimensional arrays operate on non-procedural [1] and stream models [7]. Non-procedural specifications do not have enough information to estimate accurately the memory size, since by changing the instruction sequence, large memory variations are produced. For example, assuming the code in Figure 1a is non-procedural, the memory size could vary between 100 and 150 locations, as in Figure 1b. [13] uses a data-flow oriented view, as [1], but has good results for simpler specifications (constant loop bounds, simpler indices). [12] modified the loop hierarchy and the execution sequence of the source code, by placing polyhedrons of signals derived from the operands in a common space and determining an ordering vector in that space. None of the above techniques addresses parallel specifications.

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the operand domain $a[I]$ consumes 2 array elements, and the operand domain $a[I+1]$ consumes 3. Since at most 7 out of the 10 assignments may not consume any values (the other 3 will consume at least 1 value), the maximum storage variation occurs, if the first 7 assignments generate one new value each, without consuming any, and all the consumptions occur later. Knowing from Step 2 that the memory size is 10 at the beginning of loop 2, it follows that the upper-bound of the memory size for this loop is $10+7=17$ locations. With similar reasoning, one can conclude that during the execution of this loop, the memory trace could not go below 8 locations (see Figure 5c). Thus, the bounding rectangle for this loop has the upper edge 17, and lower edge 8.

4.4 Determining the memory size range

The memory requirement for a specification is the peak of the memory trace. Since the peak of the trace is contained within the bounding rectangles (along with the whole memory trace), the highest point among all the bounding rectangles represents an upper-bound of the memory requirement. For our illustrative example, the memory requirement will not exceed 17 - the highest upper-edge of the bounding rectangles (see Figure 5c).

Since the memory size at the boundaries between the loop nests is known, the memory requirement will be at least the maximum of these values. The maximum memory size at the boundary points thus represents the lower-bound of the memory requirement. For our illustrative example, the memory requirement is higher than 15 (the lower dotted line in Figure 5c), which is the maximum of the values at the boundaries of the three loops (Figure 5a). Therefore, the actual memory requirement will be in the range [15..17]. This memory requirement range represents the result of the first pass of the algorithm. The last step of our algorithm decides whether a more accurate approximation is necessary, in such case initiating an additional pass.

4.5 Improving the estimation accuracy

If the current estimation accuracy is not satisfactory, for each loop nest whose rectangle may contain the memory trace peak (the upper edge higher than the previous memory lower-bound), a split of the iteration space is performed (by gradually splitting the range of the iterators, thus fissioning the loop nest). The *critical* rectangles corresponding to these loop nests will be replaced in a subsequent pass of the estimation algorithm by two new rectangles covering a smaller area (Figure 6a) and, therefore, following more accurately the actual memory trace, thus yielding a more accurate memory behavior analysis, and a more exact estimation. This process is iteratively repeated until a convenient estimation accuracy is reached. Figure 6a shows the refined bounding area, and 6b presents the actual memory trace for our example.

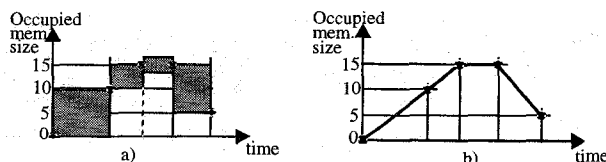


Figure 6. a) Accuracy refinement
b) complete memory trace

5. Discussion on parallelism vs. memory size

In the following we present a more complex example (Figure 7), which shows the utility of the estimation tool. This code contains a *forall* loop and multiple instructions executed in parallel (using *cobegin-coend*).

By analyzing the memory behavior of this code assuming the *forall* loop actually as a simple *for*, executed sequentially (we did not replicate the code due to lack of space), we obtain the behavior in Figure 8, and after the second pass we determine that the memory size is between [396..398].

By allowing the *forall* loop to be executed in parallel, the memory behavior becomes the one depicted in Figure 9, and the memory size is 300. Thus, the memory size for the parallel version of the code is 25% less than for the sequential case.

Having the parallel version require 25% less memory than the sequential one is a surprising result, since common sense would suggest that more parallelism in the code would need more memory. We have done some preliminary experiments in this direction, and they all seem to imply that more parallelism does not necessarily mean more memory. Moreover, we could not find (or produce) any example where the most parallel version of the code needs more memory than all the sequential versions. For most of the examples, the most parallel version had less memory requirement than most of the sequential ones. A possible explanation could be the fact that when instructions are executed in parallel, values are produced early, but also consumed early, and early consumption leads to low memory requirement. We intend to continue our work in this direction.

```
for I=0 to 97 do
  a[2*I, 0] = 0; a[2*I+1, 0] = 1;
  for J=0 to 99 do cobegin
    a[2*I,J+1]=a[2*I+1,J];
    a[2*I+1,J+1]=a[2*I,J];
  coend;
```

```
forall I=98 to 99 do
  a[2*I, 0] = 0; a[2*I+1, 0] = 1;
  for J=0 to 99 do cobegin
    a[2*I,J+1]=a[2*I+1,J];
    if (I!=99) a[2*I+1,J+1]=a[2*I,J]
    else a[2*I+1,J+1]=a[2*I,J]+a[2*I-2,J];
  coend;
```

```
for J=0 to 99 do
  for I=0 to 99 do cobegin
    a[2*I,J+101]=a[2*I+1,j+100];
    a[2*I+1,J+101]=a[2*I,J+100]+
      a[2*I,J+99];
  coend;
```

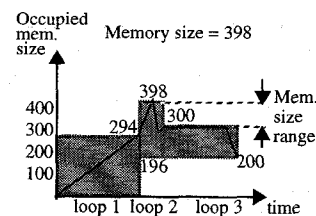


Figure 8. Memory behavior for example with simple for loop

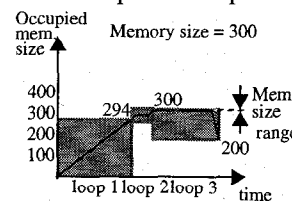


Figure 9. Memory behavior for example with *forall* loop

Figure 7. Input specification with parallel instructions

6 Experimental results

We compared our algorithm against a memory estimation tool based on symbolic execution, which assigns the signals to memory on a scalar basis to maximize sharing. We ran both algorithms on a SPARCstation 5, on 7 application kernels: image compression algorithm (Compress), linear recurrence

solver (Linear), image edge enhancement (Laplace), successive over-relaxation algorithm [8] (SOR), two filters (Wavelett, Low-pass), and red-black Gauss-Seidel method [8]. These examples are typical in image and video processing. Some of them (e.g., SOR, Wavelett, G-S) exhibit complex affine indices and conditionals.

The results of our tests are displayed in Table 1. Columns 2 and 3 show the memory requirement and the computation time obtained with the symbolic execution method. This memory size represents the optimal in terms of locations sharing. Column 4 represents the memory size estimate obtained with our algorithm (note that this is a lower-bound for the optimal value). For all the examples, the memory prediction is very close to the optimal value from column 2. The upper bound from Column 5 is used mainly as a measure of the confidence in the prediction. If this value is closer to the lower-bound estimate, the prediction is more accurate. Column 6 represents the percentile range:

$$100 * (\text{upper_bound} - \text{lower_bound}) / \text{upper_bound}.$$

Table 1: Experimental results

Application	Symbolic exec.		MemoRex algorithm			
	Optimal mem. size	Time [s]	Mem. estimate (l-b)	Upper-bound	%	Time [s]
Compress	10000	133	10000	10000	0	0.01
Linear	20002	389	20002	20002	0	0.02
Laplace	10404	87	10404	10404	0	1
SOR	38265	205	38265	38265	0	0.01
Wavelett	48003	1265	48002	72002	33	0.02
			48002	54002	11	0.15
			48002	51002	5	0.42
Low-pass	10100	384	10099	10297	1	0.27
Gauss-Seidel	13870	197	13870	13917	-0	5

The lower this value, the more confidence we can have in the estimation. For most applications, high confidence is obtained within very reasonable time. A 0 percentile range means that the lower-bound is equal to the upper-bound, producing the exact value. When there is some slack between the two, the optimal value is usually very close to the lower-bound (the memory estimate), but in worst case, depending on the memory behavior complexity, it can be anywhere within that range.

For the Wavelett example, even though we obtained a very good estimate (48002 vs. 48003) from the first pass, we needed 3 passes to reduce the percentile range and increase the confidence in the estimation, due to the complexity of the memory behavior (the memory trace inside the loops is very irregular).

7 Conclusions

We presented a technique for estimating the memory size for multidimensional signal processing applications, as part of a design space exploration environment. Different from previous approaches, we have addressed this problem considering that the algorithmic specifications written in a procedural style may also contain explicit parallel constructs. Even if the initial input does not contain explicit parallelism, partitioning and design space exploration may introduce explicit parallelism in an attempt to achieve higher performance. Our method, based on an analysis of the memory size behavior, takes into account that signals with non-overlapping lifetimes can share the same

storage locations (we assume that the assignment of arrays to the memory space is done at a later stage, and accounts for such sharing, e.g., [3]). Our experiments on typical video and image processing kernels show close to optimal results with very reasonable time. More details are available in [4].

We have also discussed some preliminary results on the influence of parallelism on the memory size, and shown that even though (parallelizing) transformations entail large variations, more parallelism does not necessarily mean more memory locations. A surprising result is that often the opposite is true. We plan to continue our research in this direction.

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