

# SYLLABUS

## CS 594 – Synthesis and Optimization of Digital Circuits

University of Illinois, Chicago  
216 TH

Spring 2005  
MWF 3:00-3:50

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### General Information

Instructor: John Lillis. email: [lillis@uic.edu](mailto:lillis@uic.edu)

Office: 936 SEO

Office Hours: TBD

Prerequisites: cs401 or eq. (cs469 or eq. recommended)

Text: **Logic Synthesis**

by S. Devadas, A. Ghosh, K. Keutzer

### Description

This class will address the so-called “logic synthesis” phase in the design of digital systems. This step takes as input a Register Transfer Level (RTL) description of a digital system (given in a high-level description language such as VHDL) and generates an implementation of the specification in a given technology. This process occurs after architectural decisions have been made (i.e., the RTL description gives a precise sequential behavior) and before physical design occurs (the topic of CS565). Given time, some architectural issues (pre-RTL) may be discussed.

### Topics (subject to change)

- Translation from High-Level Description Languages
- Combinational Synthesis
  - Two-level synthesis
  - Multi-level synthesis
- Technology mapping/library binding
- Testability of combinational circuits
- Delay analysis and optimization
  - Static timing analysis

- False path analysis
  - Optimization by gate-sizing
- Sequential analysis and optimization
  - Circuit retiming and clock scheduling
  - Finite state machine optimization
- Advanced Topics
  - Interactions with physical design
  - Architectural optimization

## Course Requirements

- Attendance and Participation (10%)
- Written Homeworks and Exams (40%)
- Paper presentation (10%)
- Implementation Project including presentation (40%)