1 Architecture/Hardware

1. The toy C program allocates a two dimensional array of integers \( m \) and then invokes a function \( \text{init\_matrix}(\text{int } **, \text{int } \) \) populates the entries in the given matrix.

Two implementations of the \( \text{init\_matrix()} \) function are given. They are semantically equivalent. However, when I use \textbf{Implementation 1}, the program runs more than 20 times faster than when we use \textbf{Implementation 2}!

Give a plausible explanation for this behavior.

```c
main () {
  int n=10000;
  int **m = (int **) malloc(n*sizeof(int *));
  int r;
  for (r=0; r<n; r++)
    m[r] = (int *) malloc(n*sizeof(int));

  init_matrix(m, n);
}

void init_matrix(int **m, int n){ // IMPLEMENTATION 1
  int i, j;
  for(i=0; i<n; i++)
    for(j=0; j<n; j++)
      m[i][j] = i*j;
}

void init_matrix(int **m, int n){ // IMPLEMENTATION 2
  int i, j;
  for(j=0; j<n; j++)
    for(i=0; i<n; i++)
      m[i][j] = i*j;
}
```
2. We say that a set of gates and constants is complete if any combinational function can be computed by a network built from only gates and constants in the set. For each of the following sets, indicate if it is complete or not.

(Note: if a constant is in the set (0 or 1), it may be used by connecting it to inputs of multi-input gates.)

(a) \{NAND\}
(b) \{AND, OR\}
(c) \{NOR\}
(d) \{XNOR, AND\}
(e) \{XNOR, AND, 0\}

3. You are designing a set-associative cache system and must decide which address bits to use for the set index. Would you choose the low order bits, high order bits, or a group of bits in the middle? Explain.

4. Draw a logic diagram (using and, or, not gates) for a 4-to-1 Multiplexer. The select lines should be labeled \(s_0, s_1\) and the data lines \(d_0...d_3\).

5. Pipelining.

(a) For a typical 5 stage pipeline, describe each stage and its function.
(b) Give one example (using pseudo assembly language) of a stall for your pipeline.
(c) Give one example (using pseudo assembly language) of a sequence of instructions with no stall.

6. What are precise interrupts and for what type of semantics are they necessary?

7. Describe where the operand is found and, where applicable, how its effective address is calculated in the following addressing modes:

(a) register:
(b) immediate:
(c) PC-relative:
(d) base or displacement:

8. A two-word relative mode branch-type instruction is stored in memory at location 207 and 208 (decimal). The branch is made to an address equivalent to decimal 195. Let the address field of the instruction (stored at address 208) be designated as \(X\). What is the value of \(X\) in binary (2s complement) using 16 bits.

(a) \text{1110 1111 0001 1000}
(b) \text{1111 1111 1111 0010}
(c) \text{1111 1111 1111 1110}
(d) \text{0000 0000 0000 0110}

9. Suppose that in a given machine design there are two cache units; one for instructions and one for data. The machine architecture prohibits self-modifying code. Which observation is most likely to be correct?

(a) the instruction cache must have “dirty” bits.
(b) the line size of the instruction cache will not be smaller than that of the data cache.
(c) the size of the data cache will be larger than that of the instruction cache.

Give a reason for your choice.

10. Consider a two-way, set-associative cache with 8192 bytes of data memory (not including the tag memory), where each cache line contains two 32-bit words (8 bytes).

(a) How many lines are in the cache?
(b) How many sets are in the cache?
(c) Show the implied address format, including the fields (and their sizes) to address the byte in the word, the word in the line, the set in the cache and the tag field.
(d) What is the size of the tag memory, in bytes?

2 Operating Systems

1. Consider the following events: trap, interrupt, system/supervisor call, procedure call.

(a) What is common among all of these events in terms of a response?
(b) What is different or unique among these events in terms of a response?

2. Briefly (one or two simple sentence), but specifically, explain what it means for a process to be in each of the following states: running, blocked, ready, terminated.

3. Consider virtual memory system where a page map table contains 512 entries and each entry in the table is 16 bits, including the valid/invalid bit.

(a) If the page size is 1024 bytes, how many bits of a physical address are used to specify the page frame number?
(b) How many bits of a physical address are used to specify the displacement or offset within the page frame?

4. Assume we have two binary semaphores S and T with initial values of 0 and 1, respectively. If the following semaphore operations execute in the order shown (by various unnamed processes), what are the values of the semaphores S and T at the end of the sequence? Note: The P and V operations are sometimes called Wait and Signal, respectively. Assume that a P operation checks the value of the semaphore before changing the value.

\[
P(S), P(S), P(S), V(S), P(T), V(S)
\]

\[
V(S), P(S), V(T), V(T), P(S), V(T)
\]

5. Consider a multiprogrammed (timeshared) OS with a time slice (quantum) of 5 units and the following set of processes. Assume that the CPU scheduling is done round robin meaning first P1, then P2, then P3, then P1, etc.

- P1 requires 18 units of CPU time in total, but makes an I/O request after using 7 units of time. The I/O operation requires 10 units of time.
- P2 requires 7 units of CPU time and no I/O time
- P3 requires 3 units of CPU time and no I/O time
Ignoring all overhead time (time associated with OS execution), clearly show on a timeline when each process is dispatched.

6. Deadlock.
   (a) Describe the four necessary and sufficient conditions for deadlock.
   (b) For each of the four conditions you enumerated in (a), describe a way of avoiding deadlock by denying that condition.

7. Processes.
   (a) Describe the requirements necessary to support the process abstraction.
   (b) How would those requirement be implemented in an operating system?

3 Networks

1. Explain the operation of the Network Address Translation (NAT) function. Consider both cases: sending and receiving data.

2. Explain the silly window syndrome that occurs in TCP, and how it can be dealt with.

3. A large number of IP addresses are available starting at 198.16.0.0. Organizations A,B,C,D request for 4000, 2000, 4000, 8000 addresses, respectively, in that sequential order. For each request, give the first IP address assigned, the last IP address assigned, and the mask in w.x.y.z/s notation.

4. Explain the differences between the selective repeat and go-back-n protocols for data transmission.

5. Congestion Control.
   (a) What is the purpose of the van Jacobson congestion control algorithm and what does it depend on to be effective?
   (b) How does van Jacobson work?

   (a) What does the link-state protocol do?
   (b) Sketch the algorithm for the link-state protocol.

7. How is a fully qualified domain name, such as cs.uic.edu, translated into an IP number?