Milos Hrkic

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Education

The University of Illinois at Chicago (UIC)
PhD in Computer Science
GPA: 5.00 (A=5.00), degree awarded July 2004

The University of Illinois at Chicago (UIC)
Bachelor of Science in Computer Science
GPA: 4.96 (A=5.00), degree awarded May 2000

Experience

IBM Microelectronics - EDA, East Fishkill, NY, September 2004 - present
Advisory Software Engineer, September 2004 - present: EDA software development on routing based optimization.

Synplicity, Sunnyvale, CA, August 2004
Consultant: tested and evaluated methods for timing optimization of FPGAs by placement-coupled logic replication.

IBM Austin Research Laboratory, May-August 2001, 2002 and 2003
Technical Co-op, May-August 2003: developed and tested new congestion aware and cost/performance driven algorithms for interconnect synthesis and buffering. Implemented fast porosity and buffer aware fan-out tree embedding algorithm. Devised and implemented new porosity aware wire segmenting scheme for van Ginneken style buffer insertion. Algorithms incorporated into Chipbench and PDS tools.
Co-op Pre-Professional Programmer, May-August 2002: developed and tested blockage avoidance algorithms for interconnect synthesis and buffering. Developed and tested cost aware version of van Ginneken style buffering algorithm. Implemented internal debugging tool for visualizing debug level output of Chipbench and PDS tools.
Co-op Pre-Professional Engineer, May-August 2001: developed and tested timing driven algorithms for interconnect synthesis and buffering. Performed run-time/solution quality evaluation of various interconnect synthesis algorithms (C-Tree, P-Tree, S-Tree).

The University of Illinois at Chicago, CS department, September 1998 - July 2004
Research Assistant, May 2000 - July 2004: research and development of tree optimization algorithms. Developed and implemented universal tree synthesis and optimization package (U-Tree). Developed and implemented a set of buffered tree synthesis and optimization algorithms with consideration of spatial and temporal locality, sink polarity requirements, solution cost, congestion and blockages (S-Tree, P-Tree, SP-Tree). Developed placement-coupled logic replication algorithm and implemented a tool for timing optimization of FPGAs.
Undergraduate Research Assistant, May 1999 - May 2000: implemented permutation constrained blockage aware performance driven algorithm (P-Tree) for interconnect synthesis with graphic user interface (presented at SIGDA University Booth at DAC 2000).
Computer lab consultant, September 1998 - May 1999: provided technical support to students

Petnica Science Center, Yugoslavia, 1993-1997
Junior Research Assistant / Lecturer: lectured on selected topics in computer science and computer engineering (high school level), assisted with student research projects.

Freelance Computer Programmer, Belgrade, Yugoslavia, 1990-1998
Developed and implemented various database applications, computer hardware control software, maps and graphics applications, teaching aid software.

Awards

IBM PhD Fellowship, IBM Corporation, 2003-2004
University Fellowship, The University of Illinois at Chicago, 2002-2003
CADAthlon Programming Contest at ICCAD, Second place, San Jose, CA 2002
EECS Senior Scholar Award, The University of Illinois at Chicago, 2000
EECS Merit Scholar Award, The University of Illinois at Chicago, 1999
Scholarship awarded by Studenica Foundation, San Rafael, CA, 1998-2000
Dean's List certificate, The University of Illinois at Chicago, Fall 1998, Spring 1999, Fall 1999, Spring 2000

Patents

- J. Lillis, M. Hrkic
Placement-Coupled Logic Replication
University of Illinois Disclosure 60/575250 (US patent pending)

- C.J. Alpert, M. Hrkic, S.T. Quay
Method and Apparatus for Performing Density-Based Buffer Insertion in an Integrated Circuit Design
United States Patent 7,137,081 (IBM)

- C.J. Alpert, M. Hrkic, J. Hu, S.T. Quay
Method and Apparatus for Generating Steiner Trees Using Simultaneous Blockage Avoidance, Delay Optimizations and Design Density Management
United States Patent 7,127,696 (IBM)

- C.J. Alpert, C-N. Chu, R.G. Gandham, M. Hrkic, J. Hu, C. Kashyap, S.T. Quay
Apparatus and method for incorporating driver sizing into buffer insertion using a delay penalty estimation technique
United States Patent 6,915,496 (IBM)

Journal publications

- M. Hrkic, J. Lillis, G. Beraudo
An Approach to Placement-Coupled Logic Replication
IEEE Transactions on Computer-Aided Design, vol. 25, no. 11, November 2006, pp. 2539-2551

- C.J. Alpert, C-N. Chu, R.G. Gandham, M. Hrkic, J. Hu, C. Kashyap, S.T. Quay
Simultaneous Driver Sizing and Buffer Insertion Using a Delay Penalty Estimation Technique
IEEE Transactions on Computer-Aided Design, vol. 23, no. 1, January 2004, pp. 136-141

- M. Hrkic, J. Lillis
Buffer Tree Synthesis with Consideration of Temporal Locality, Sink Polarity Requirements, Solution Cost, Congestion and Blockages
IEEE Transactions on Computer-Aided Design, vol. 22, no. 4, April 2003, pp. 481-491

- C.J. Alpert, G. Gandham, M. Hrkic, J. Hu, A.B. Kahng, J. Lillis, B. Liu, S.T. Quay, S.S. Sapatnekar, A.J. Sullivan
Buffered Steiner Trees for Difficult Instances,
IEEE Transactions on Computer-Aided Design, vol. 21, no. 1, January 2002, pp. 3-14

Conference publications

- Hosung Kim, J. Lillis, M. Hrkic
Techniques for improved placement-coupled logic replication
Proc. 16th Great Lakes Symposium on VLSI, Philadelphia, May 2006

- M. Hrkic, J. Lillis, G. Beraudo
An Approach to Placement-Coupled Logic Replication
Proc. 41st Design Automation Conference, San Diego, June 2004

- C.J. Alpert, M. Hrkic, J. Hu, S.T. Quay
Fast and Flexible Buffer Trees that Navigate the Physical Layout Environment
Proc. 41st Design Automation Conference, San Diego, June 2004

- M. Hrkic, J. Lillis
Addressing the Effects of Reconvergence on Placement-Coupled Logic Replication
Proc. 13th International Workshop on Logic and Synthesis, Temecula, CA, June 2004.

- C.J. Alpert, M. Hrkic, S.T. Quay
A Fast Algorithm for Identifying Good Buffer Insertion Candidate Locations
Proc. ACM International Symposium on Physical Design, April 2004.

- C.J. Alpert, G. Gandham, M. Hrkic, J. Hu, S.T. Quay
Porosity Aware Buffered Steiner Tree Construction
Proc. ACM International Symposium on Physical Design, April 2003.

- M. Hrkic, J. Lillis
S-Tree: A Technique for Buffered Routing Tree Synthesis
Proc. 39th Design Automation Conference, New Orleans, June 2002.

- M. Hrkic, J. Lillis
Buffer Tree Synthesis with Consideration of Temporal Locality, Sink Polarity Requirements, Solution Cost and Blockages
Proc. ACM International Symposium on Physical Design, April 2002.

- C.J. Alpert, C-N. Chu, R.G. Gandham, M. Hrkic, J. Hu, C. Kashyap, S.T. Quay
Simultaneous Driver Sizing and Buffer Insertion Using a Delay Penalty Estimation Technique
Proc. ACM International Symposium on Physical Design, April 2002.

- M. Hrkic, J. Lillis
S-Tree: A Technique for Buffered Routing Tree Synthesis
Proc. 10th Workshop on Synthesis and System Integration of Mixed Technologies, Nara, Japan, October 2001.

- C.J. Alpert, M. Hrkic, J. Hu, A.B. Kahng, J. Lillis, B. Liu, S.T. Quay, S.S. Sapatnekar, A.J. Sullivan, P.Villarrubia
Buffered Steiner Trees for Difficult Instances
Proc. ACM International Symposium on Physical Design, April 2001.